



Exhibit A

Cisco Reference

In-house Documentation

Submitted for review on 4/12/99

RECEIVED

JAN 20 2004

Technology Center 2600

November 7, 2003

OC-192 Very Short Reach Interconnect Module Product Specification: ENG-48278, Rev. 0.3



Document Number

ENG-48278

Revision

0.3

Author

Mark Nowell

Project Manager

Doug Knight

OC-192 Very Short Reach Interconnect Module

Product Specification

RECEIVED

JAN 20 2004

Technology Center 2600

Project Headline

This document defines the specifications for a very short reach (VSR) parallel optics transceiver module designed to interconnect equipment transmitting OC-192 SONET frames.

Reviewer

Name	Acceptance Date	Name	Acceptance Date
Mark Nowell	Apr. 23, 1999	Doug Knight	Apr. 23, 1999
HW Design Engineer		HW Design Eng Manager	
Name	Date	Name	Date
FW Design Engineer		FW Design Eng Manager	
Name	Date	Name	Date
SW Design Engineer		SW Design Eng Manager	
Name	Date	Name	Date
Development Test Engineer		Development Test Manager	
Name	Date	Name	Date
Product Test Engineer		Product Test Manager	
Name	Date	Name	Date
Compliance Engineer		Mechanical Engineer	
Name	Date	Name	Date
Manufacturing Engineer		CA Representative	
Name	Date	Name	Date
Engineering Director		VP Engineering	

A printed version of this document is an uncontrolled copy.

Modification History

Rev	Date	Originator	Comment
0.1	April 12, 1999	Mark Nowell /Roger Li/Gary Nicholl/Jean-Yves Ouellet	Initial Release
0.2	April 23, 1999	Mark Nowell /Roger Li/Gary Nicholl/Jean-Yves Ouellet	Contains changes after initial review
0.3	June 8, 1999	Mark Nowell	Add error detection. Fix typos. Change Pin-out.

1.0 Overview

The OC-192 VSR transceiver module is a transmit and receive electro-optic device used to provide a low-cost physical layer interconnect for OC-192 based systems. It is our intent that the module contains parallel optical transmit and receive sub-modules as well as a converter chip that will ensure byte and channel alignment and interface between the optical sub-modules and a designed OC-192 framer chip. The minimum target distance for this transceiver module is 200m on 62.5/125 μ m multimode fiber (62MMF) and 500m on 50/125 μ m multimode fiber (50MMF).

The application for this module is for a low-cost router to router interconnection within an office. Additionally, this may be used to interconnect a router with a DWDM terminal where only short distance links are necessary.

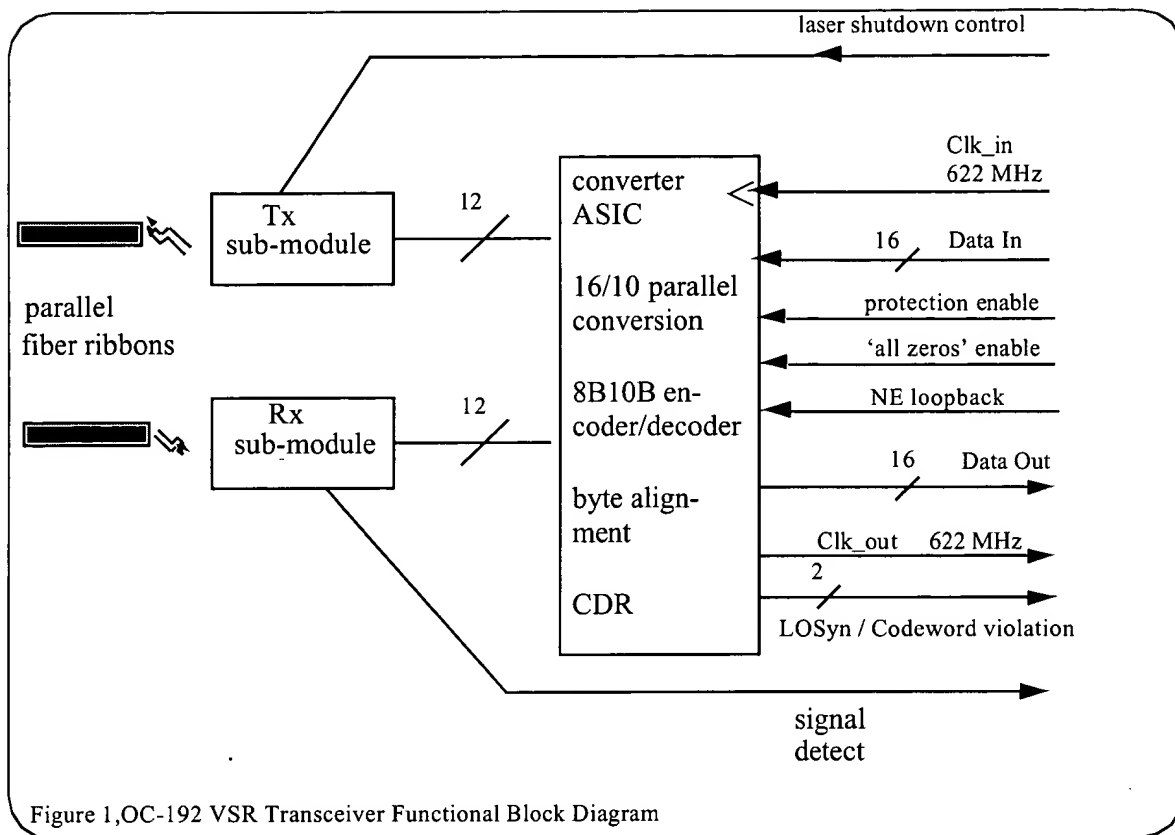
Note: This specification assumes a solution based on short-wavelength VCSEL based parallel optics. There are other potential solutions such as long-wavelength based parallel optics or long-wavelength high speed serial transmission. The specifications in this document were adopted because it was felt that this technology was the most likely to meet Cisco's availability/price/size requirements. However, if other solutions can be shown to meet the functional requirements as well as the availability/size/price requirements specified in this document, a counter proposal may be considered.

2.0 High-Level Description

The OC-192 VSR transceiver module is a bi-directional device with a transmitter and receiver in the same physical package. The module interfaces to the user world via a connector interface on the electrical ports and an MTP (MPO) connector interface on the optical ports. A schematic of the VSR module functional block diagram is illustrated in Figure1, "OC-192 VSR Transceiver Functional Block Diagram".

In the transmit direction, the transceiver module receives a 16-bit 622 Mb/s LVDS electrical signal from the OC-192 framer chip. A converter chip transforms the 16 bit parallel bus to 10 parallel channels. The converter chip generates two additional channels. One channel is a 'protection' channels created by performing an XOR operation on the 10 data channels. If any of the ten channels fail, the data can be recovered at the receiver from the protection channel. The final channel carries a set of CRC's for each of the other 11 channels. This channel is used to determine whether any errors occurred during transmission. Each channel is 8B/10B encoded and some SONET framing bytes on each channel are overwritten with a frame marker consisting of characters defined for the 8B/10B code [1]. The purpose of the frame markers is to aid the de-skewing circuitry at the receiver. The 12 channels are passed to the optical transmitter module which transmits the data along the 12 optical fibers in the ribbon fiber at a bit rate of 1.244 Gb/s per channel. The transceiver module shall synthesize the required high speed clock from the 622MHz input clock. The transmit data interface is forward timed.

In the receive direction, the transceiver module receives 12 parallel optical signals on a fiber ribbon with an MTP (MPO) connector. Each channel is operating at 1.244 Gb/s. The optical sub-module converts the signal to an electrical equivalent and it is then transmitted to a converter chip. The converter chip shall recover the clock and 8B/10B decode on each channel. It will then de-skew the individual channels, by using the frame markers as delimiters, to compensate for any inter-channel skew that may occur due to propagation delay differences in the transmit and



receive optical sub-modules as well as the fiber ribbon. The converter chip will then transform the 10-bit wide data to 16-bit wide data and replace the SONET framing bytes previously removed. The converter chip will auto-detect whether the ribbon fiber patchcord has a crossover and will internally account for this to ensure correct data byte ordering at the output.

If the converter chip detects a loss of synchronisation (LOSyn) on any single channel within the 10 data channels, it will recover that channel from the protection channel. If it detects LOSyn from more than one channel in the group of 10, it will overwrite the output of all channels with all zeros until valid data is transmitted and synchronisation is achieved (this feature can be disabled). Additionally, the receiver calculates the CRCs for blocks of data on each channel. If the calculated CRC does not match the corresponding transmitted CRC, an error is assumed to have occurred and the errored block is replaced by extracting it from the protection channel. The converter chip shall provide a 16 bit parallel 622 Mb/s LVDS signal for connection to the OC-192 framer chip retimed with a 622 MHz output clock.

The modules will be optically connected with MTP (MPO) terminated 12 fiber ribbon cables. These are available from a number of vendors. The MTP(MPO) connector is specified in [2].

2.1 Performance

The VSR transceiver module will transmit OC-192 frames over 200m (min.) of 62MMF ribbon or 500m (min.) of 50MMF ribbon. The module will compensate for any inter-channel skew that occurs within the link and will interface directly to an OC-192 framer chip. The module will operate with a target BER of $< 10^{-15}$.

2.2 Functional Blocks

The VSR transceiver module consists of 3 functional blocks:

A printed version of this document is an uncontrolled copy.

- Optical transmit sub-module
- Optical receive sub-module
- converter chip

The converter chip acts as an interface between the OC-192 framer chip and the optical sub-modules. The converter chip's purpose is to adapt the incoming signals into a format that allows them to be transmitted on a parallel optic link and realigned after transmission. There are separate optical sub-modules for transmit and receive. Each optical sub-module interface connects to an MTP (MPO) connectorised fiber ribbon. More details will be given of the functional blocks in Section 3.0 on page8. The interface specifications for the module will be given in the next section.

2.3 Module I/O specifications

2.3.1 Optical interface specifications

The OC-192 VSR interconnect module's optical interface shall meet the specifications given in Table1, "Optical Interface Specifications". The specifications assume modal bandwidths of 160 MHz.km for 62MMF and 500 MHz.km for 50MMF.

Table 1: Optical Interface Specifications

Parameter	Min.	Max	Units	Notes
Transmitter module^{a, b}				
P_{out}	-10	-6	dBm	^c
λ_c	830	860	nm	
Optical Extinction ratio	6		dB	
$\Delta\lambda_{rms}$		0.85	nm	
t_{rise}/t_{fall} (20-80%)		260	ps	
RIN		-116	dB/Hz	
Systematic Jitter contribution		160	ps _{p-p}	
Total jitter contribution		345	ps _{p-p}	
Receiver Module^d				
P_{in}	-18	-6	dBm	^e
λ_c	830	860	nm	
Return loss	12		dB	
Signal detect - asserted		-19	dBm	
Signal detect -de-asserted	-26		dBm	
Signal detect hysteresis	1	4	dB	

a. all transmitter specifications are per channel and are measured at the end of a 2m patchcord.

b. in the event of accidental transmitter to transmitter connection, no damage shall occur that will prevent the continued operation of the transmitter module within specification.

- c. output power for the ribbon will be compliant with FDA Class 1 and IEC Class 3A eye safety requirements (all channels aggregated).
- d. all receiver specifications are per channel.
- e. Receiver sensitivity shall be such that the $BER \leq 10^{-15}$ with the minimum optical power including the optical path penalty (includes 1.5dB loss for connectors).

2.3.2 Data Bit Ordering

The data bit ordering shall be as illustrated in Figure 2. The MSB of the first SONET byte shall appear on pin D15 and the LSB of the next SONET byte shall appear on pin D0. The data bit ordering on the parallel optical fiber will be described in more detail in Section 3.3 on page 8. The converter chip fills the channels with successive bytes of the SONET frame so that the first byte is transmitted on channel #1 and the second byte is transmitted on channel #2 etc. A diagram showing the transmission format is shown in Figure 8, "Parallel Serial Links: Transmission Format". The description of the protection links and the alignment delimiters will be described in more detail in Section 3.3 on page 8.

The MTP (MPO) connector is a keyed connector as described in [2]. However, the patchcord assembly may be terminated so the fiber ribbon either connects back to back or else with a 180° twist. This results in a potential reversal of order of the input fiber channels depending on which version of patchcord is used. To be tolerant to this, the converter chip shall use different frame delimiters to delimit links 1-6 and links 7-12. In the receive path, the converter chip will then detect the polarity of the patchcord and adjust accordingly so that the correct data bit ordering occurs at the module output interface.

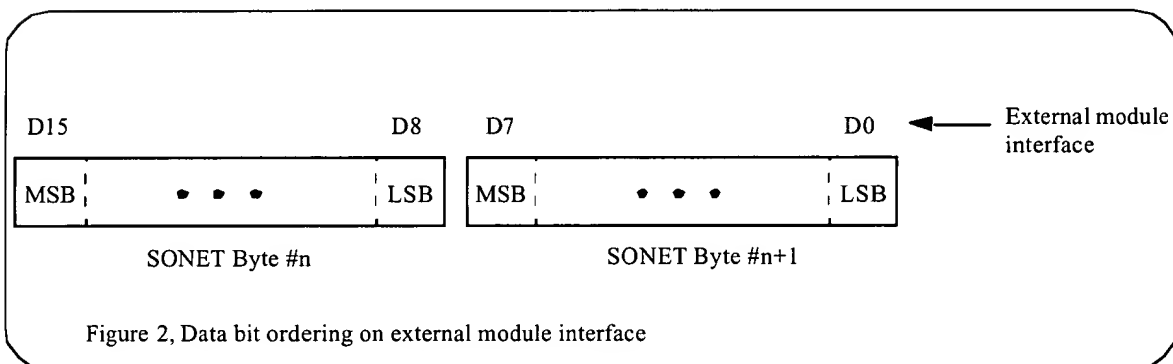


Figure 2, Data bit ordering on external module interface

2.3.3 Module Electrical I/O specifications

The electrical I/O specifications of the module's electrical interface shall conform to the specifications given in Table 2, "Module electrical I/O specifications". The data signals shall be LVDS format and the non-data signals shall be LVTTTL.

Table 2: Module electrical I/O specifications

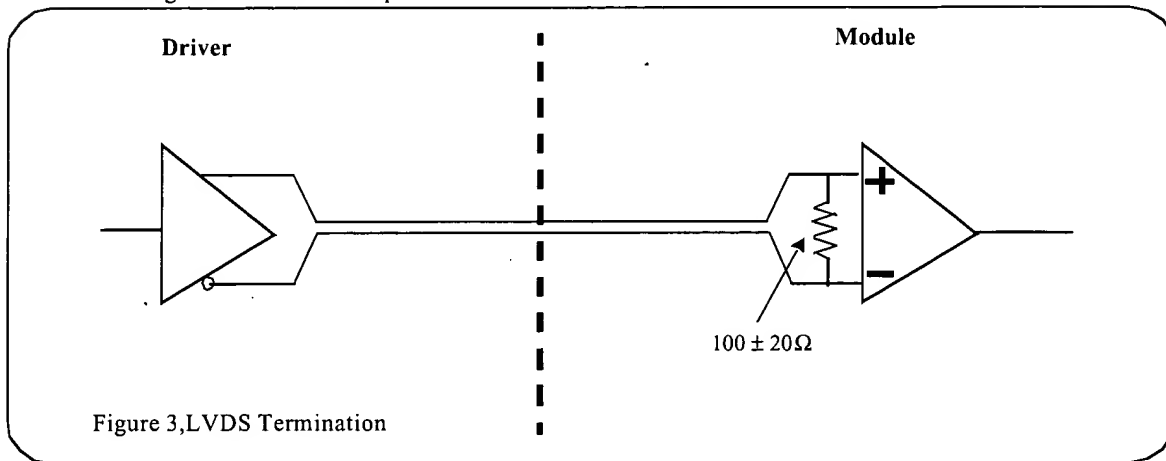
Parameter	Min.	Typ.	Max	Units	Notes
Supply voltage	2.97	3.3	3.63	V	
Power consumption			7	W	
Clk_in	622.08-100ppm		622.08+100ppm	MHz	
Clk_in duty cycle	40		60	%	
Input return loss (clock)	15			dB	^a
Input return loss (data)	15			dB	^a
LVDS input differential voltage	308	380	456	mV	
LVDS input high voltage	1320	1440	1550	mV	
LVDS input low voltage	970	1060	1150	mV	
Clk_out	622.08-100ppm		622.08+100ppm	MHz	
Clk_out duty cycle	45		55	%	
LVDS output differential voltage	308	380	456	mV	
LVDS output offset voltage	1148	1246	1353	mV	
LVDS output high voltage	1075		1780	mV	
LVDS output low voltage	650		825	mV	
LVDS rise/fall time	200		350	ps	
V _{oh}	2.0			V	
V _{ol}			0.8	V	
V _{ih}	2.0			V	
V _{il}			0.8	V	
Output Total Jitter			100	ps _{p-p}	^b

a. Return loss shall be better than the specified value from 10 MHz to 1 GHz.

b. Cycle to cycle jitter on receive clock. The jitter specifications are expected to be similar to Gigabit Ethernet [1].

2.4 LVDS termination

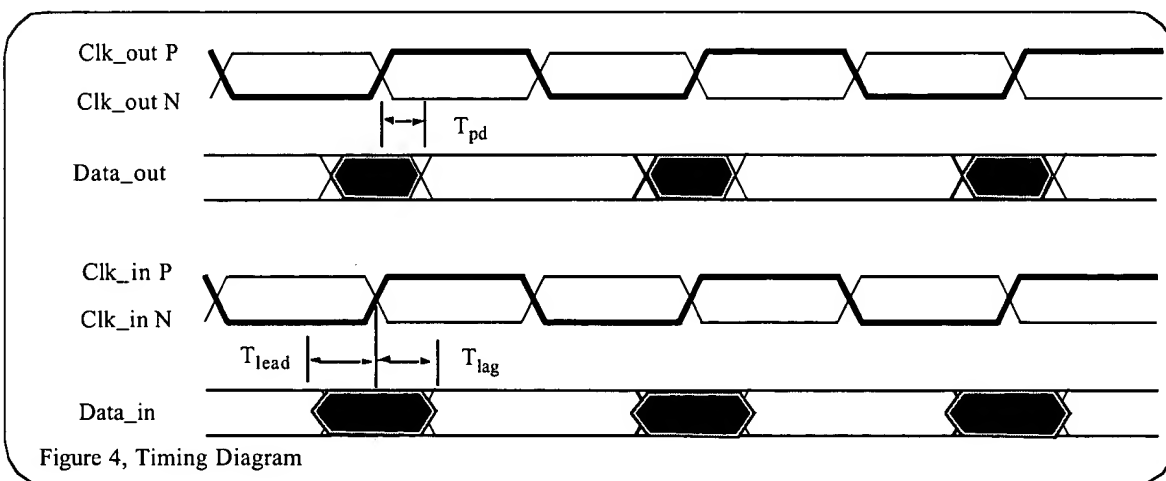
The LVDS termination shall be as illustrated in Figure 3, "LVDS Termination". It is assumed that the chip interfacing with the module outputs has similar termination.



2.5 AC Electrical Characteristics

Table 3: AC Electrical Characteristics

Symbol	Parameter	Min.	Typical	Max	Unit
T_{pd}	Receiver data propagation delay with respect to the rising edge of Clk_out	600		1000	ps
T_{lead}	Transmitter input data leading the rising edge of Clk_in			600	ps
T_{lag}	Transmitter input data lagging the rising edge of Clk_in			600	ps



A printed version of this document is an uncontrolled copy.

3.0 Detailed Description

3.1 Optical transmit sub-module

The optical transmit sub-module shall meet the optical specifications stated in Table 1, "Optical Interface Specifications". The connector interface shall be a standard MTP (MPO) ribbon fiber connector. The optical transmit sub-module shall be capable of transmitting on 12 parallel fibers. Fiber #1 shall be designated as the right-most fiber when looking into the optical connector interface. The optical transmit sub-module shall provide a control input to allow all the lasers to be enabled or disabled.

3.2 Optical receive sub-module

The optical receive sub-module shall meet the specifications stated in Table1, "Optical Interface Specifications". The connector interface shall be a standard MTP (MPO) ribbon fiber connector. The optical receive sub-module shall be capable of receiving signals from 12 parallel fibers. Fiber #1 shall be designated as the right-most fiber when looking into the optical connector interface. The optical receive sub-module shall provide a control output to show whether an optical AC signal is present. The photo-detector diameters shall be large enough to fully detect the transmitted light from the largest supported fiber type (62MMF).

3.3 Converter chip

The converter chip is an ASIC designed to interface between the OC-192 framer chip and the optical sub-modules. A functional schematic of the chip is given in Figure6, "Schematic diagram of converter chip". The converter chip utilises some codewords defined in [1] for frame delimiters. For reference, the specific characters used in the frame delimiters are shown in Table4, "8B/10B code groups used in frame delimiter"

Table 4: 8B/10B code groups used in frame delimiter

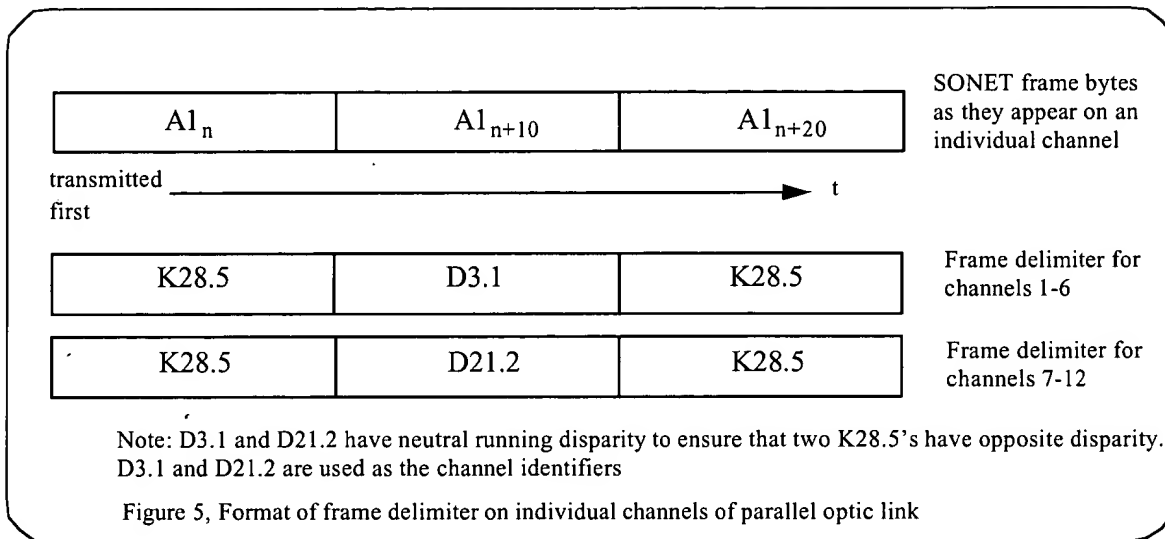
Code group name	Octet Value	Current RD-	Current RD+
		abcdei fghj	abcdei fghj
K28.5	BC	001111 1010	110000 0101
D3.1 ^a	23	110001 1001	110001 1001
D21.2 ^a	55	101010 0101	101010 0101

a. both D3.1 and D21.2 have neutral mark/space density.

3.3.1 Transmit Direction

In the transmit direction, the 16 bit wide LVDS signal at 622 Mb/s from the external SONET framer chip passes into a framer and byte demultiplexer block. In this block the SONET frame delimiters are determined so that a framing pulse can be generated. A schematic of the framer and byte demultiplexer block is illustrated in Figure7, "Framer and Byte Demux schematic".

The 10 demultiplexed bytes are then forwarded on to the 8B/10B encoders. In parallel the data from channels 1-10 are XORed together to form channel 11. The frame delimiters are not XORed as shown in Figure8.



The 12th channel is called the “Error Correction Channel” (ECC). This channel carries CRC information for the other 11 channels that the receiver can use to detect and correct transmission errors. The data in each channel is divided into ‘virtual blocks’ that are 24 bytes long. The first virtual block of a frame is aligned with the frame delimiter to ensure consistent wrap-around. A 16-bit CRC is calculated for each virtual block in each channel. The 11 16-bit CRCs are then transmitted serially in the ECC. The final two bytes of the ECC channel’s virtual block contain its own 16-bit CRC calculated over the other eleven 16-bit CRCs.

The format of the ECC is illustrated in Figure 9, “Error Correction Channel Format - Composition of 24 Byte virtual block”. For the case where the virtual blocks contain the frame delimiter, no CRC’s will be calculated. Instead the virtual block on the ECC will contain the frame delimiter bytes and the rest of the block will be filled with SONET A1 bytes.

All 12 channels are 8B/10B encoded. If a frame pulse is present, the first three SONET A1 bytes on each channel are overwritten with codewords that form a frame delimiter that the receiver will recognise. The frame delimiters for channels 1-6 and channels 7-12 are different to allow detection of the polarity of the patchcord (and therefore channel order) at the receiver. The frame delimiter is shown in Figure 5.

As shown in Figure 5, the first A1 is overwritten by a K28.5, the second A1 is overwritten by D3.1 or D21.2 depending on the channel number and the third A1 is overwritten by a K28.5. Because of the neutral running disparity of the second codeword of the delimiter, the K28.5 in the third codeword of the delimiter shall have the opposite running disparity to the first. This ensures that one comma will be inserted at the beginning of each frame. The 10 bit wide data channels are then forwarded to the transceiver blocks that serialise the data into a 1.244Gb/s LVDS output signal that interfaces directly to the optical transmit sub-module. A schematic of the transmission format on the parallel serial links is illustrated in Figure 8, “Parallel Serial Links: Transmission Format”. The internal 124.4 MHz and 1.244 GHz are synthesized from the input 622.08 MHz clock.

3.3.2 Receive Direction

In the receive direction, the 12 1.244 Gb/s parallel LVDS signals are received from the optical receive sub-module by the transceiver blocks. The transceiver blocks perform clock and data recovery and deserialise each data channel into a 10-bit wide data path. Comma detection and 10-bit character alignment should be enabled only when LOSyn has been detected on the corresponding link.

The 12 channels then are 8B/10B decoded. The 8B/10B decoder blocks monitor for the frame delimiter sequence and forward a frame marker signal to the alignment blocks to indicate the presence and position of the frame delimiter. The 8B/10B decoder block also detects the polarity of the incoming channels. If the polarity of the channels is reversed (e.g. D3.1 appears within the frame delimiter on channels 7-12) then a signal is forwarded to the byte multiplexer to reverse the channel order. The state diagram for detection of the frame delimiter is illustrated in Figure 11. In order to prevent spurious frame delimiters caused by transmission errors resulting in re-framing, a prediction algorithm using a counter shall be used to predict the location of the frame delimiters. The state diagram for this algorithm is shown in Figure 12.

The 8B/10B decoder block also detects codeword violations and asserts a control signal that is available for test purposes (duration 50ns). The data passes through an alignment buffer that uses an elastic store to align the 12 data channels using the alignment control signal made available by the 8B/10B decoder block.

The frame delimiter bytes are overwritten with the A1 framing bytes. The transceiver blocks generate the 124.4 MHz clocks. These clocks drive the internal channel buses. The master clocking of the read side of the alignment buffers is done using one of these internal 124.4 MHz clocks as the master clock. The master clock shall be from one of the two innermost channels (6 or 7). The 622.08 MHz clock is synthesized from the 124.4 MHz internal clock with a x5 PLL. The decoded data is then multiplexed into 16-bit wide 622 Mb/s LVDS signal.

In the 8B/10B decoder, a loss of synchronisation (LOSyn) algorithm will detect whether each channel has lost synchronisation and is no longer transmitting valid data. If one decoder within one of the 10 data channels detects LOSyn, it will send a control signal to the byte multiplexer block to indicate that there is a LOSyn condition on one channel and that the data for this channel should be recovered from the extra XORed protection channel. If more than one channel in the group exhibits LOSyn then the output of the byte demultiplexer shall overwrite all data in all channels with 'zeros' until the LOSyn signal is cleared.

The LOSyn algorithm is based on looking for 8B/10B codeword violations within blocks of 4 codewords (codeblock). If any violation occurs within a block of 4 codewords, this is considered an invalid codeblock by the state machine. The state machine of the LOSyn procedure is illustrated in Figure 10, "Loss of Synchronisation procedure (state diagram)". The converter chip shall have two control pins to make both the protection switching optional and the 'all zeros' optional.

The converter chip also performs error correction by using the 16-bit CRCs transmitted in the ECC. The error correction is performed in the byte multiplexer block after all the channels are aligned. The 16-bit CRC for the virtual block on the ECC is calculated first, if it matches transmitted CRC, then the ECC virtual block is assumed to be error free allowing error correction to be performed. The 16-bit CRC is then calculated for the protection channel virtual block. Again if it matches the transmitted CRC then error correction can then be performed on the 10 data channels. If an error is detected in either the protection channel or ECC, no further error correction can be performed on that virtual block. If no errors are detected, the 16-bit CRC is calculated for each of the ten data channels. If an error is found in a channel, the errored virtual block is replaced by extracting the correct data from the protection channel. If more than one data channel is determined to have an error in the same virtual block, then no error correction is performed. Finally, if a virtual block contains the frame delimiters, no error correction is performed. (It is assumed that the BER on each channel is $< 10^{-12}$ and that the errors are uncorrelated between channels).

The converter chip shall also provide the ability to perform near-end local loopback (Tx to Rx) for testing purposes.

3.3.3 Converter Chip Features

The main features of the converter chip are:

- Skew tolerance of at least 200ns.
- Auto detection and compensation for channel reversal due to optical patchcord polarity to ensure correct bit ordering at module output.
- Redundant protection channels to make link robust to single channel failures (may be disabled).

A printed version of this document is an uncontrolled copy.

- Error correction based on 16-bit CRC
- Loss of synchronisation algorithm to detect failing channel.
- All 'zeros' generation when loss of synchronisation detected on more than one channel within a group (may be disabled).
- Loss of synchronisation control signal (asserted during duration of LOSyn state).
- Single codeword violation control signal (duration 50ns).
- local loopback (near-end loopback Tx-Rx).
- LVDS interface for data signals.
- LVTTTL interface for control signals.

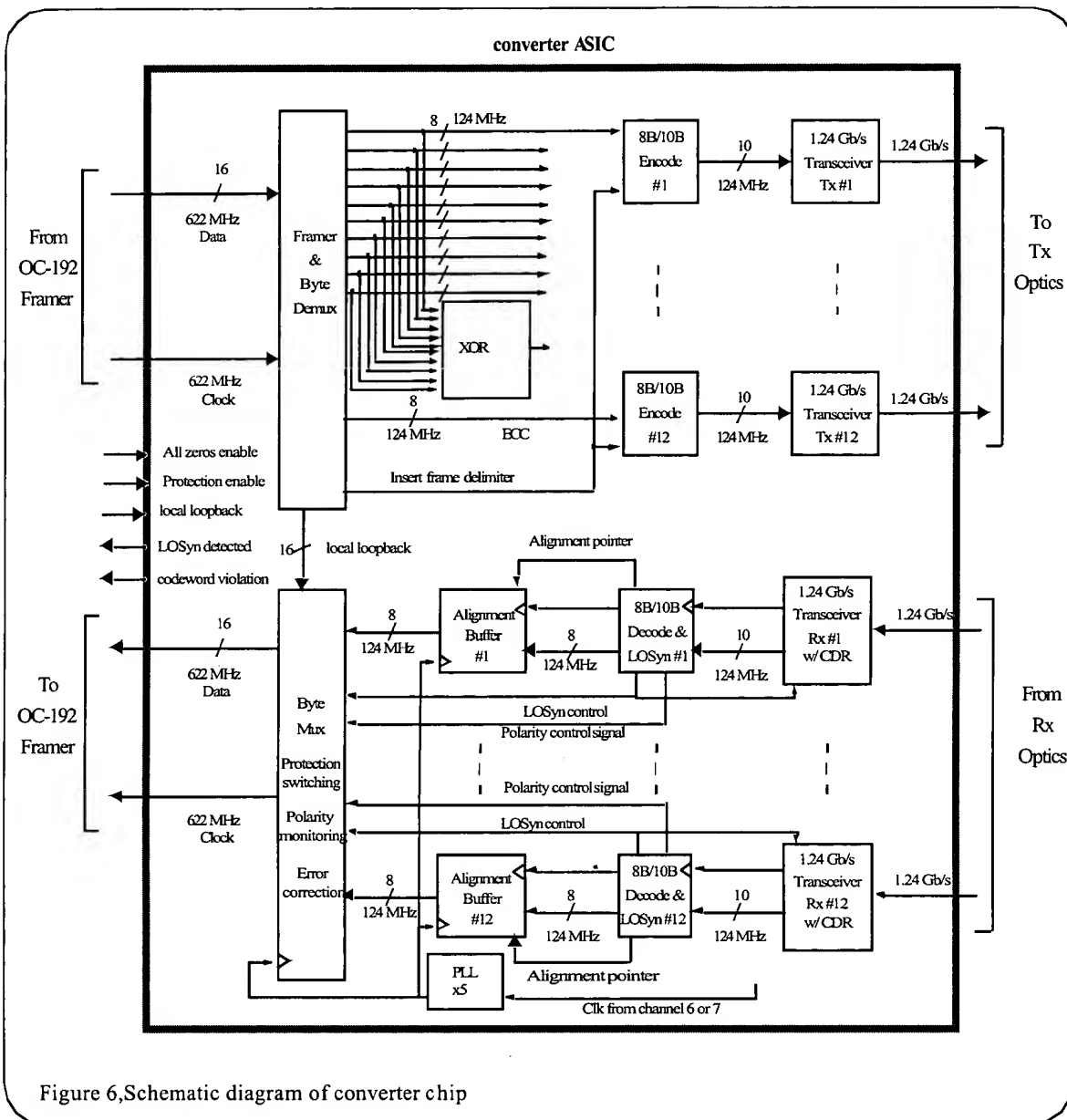
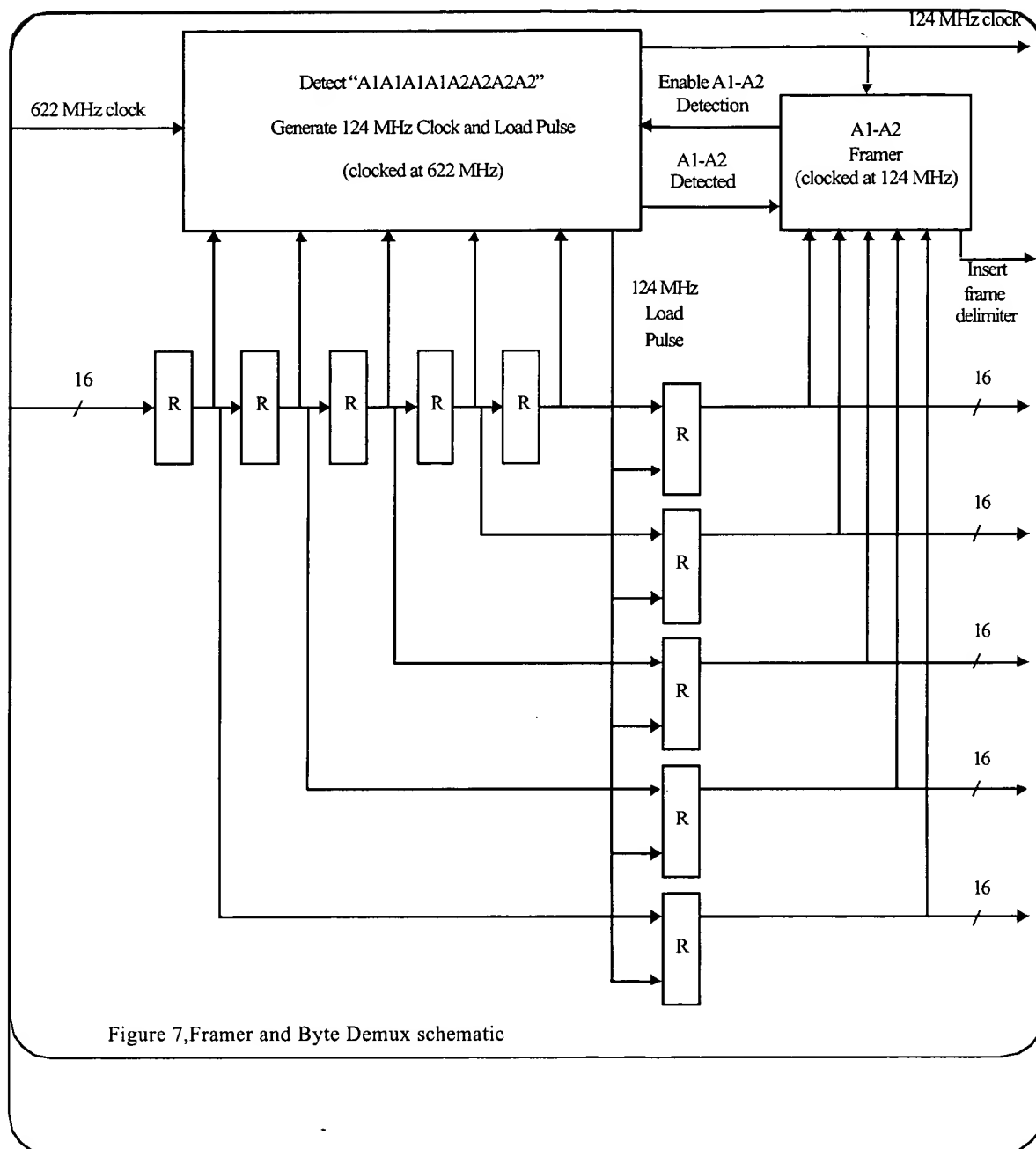
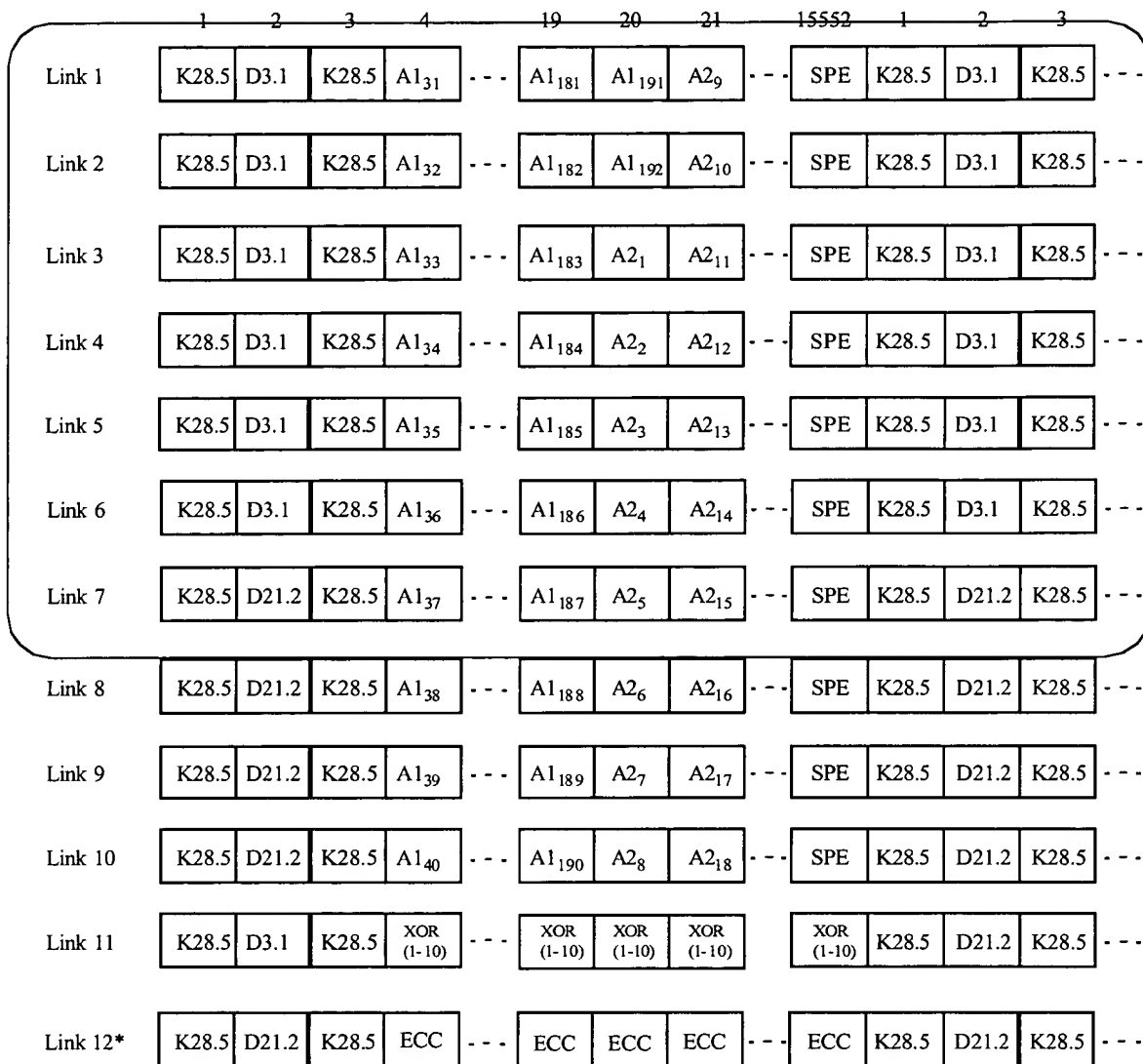


Figure 6, Schematic diagram of converter chip





* See Figure 9 for ECC format

Figure 8, Parallel Serial Links: Transmission Format

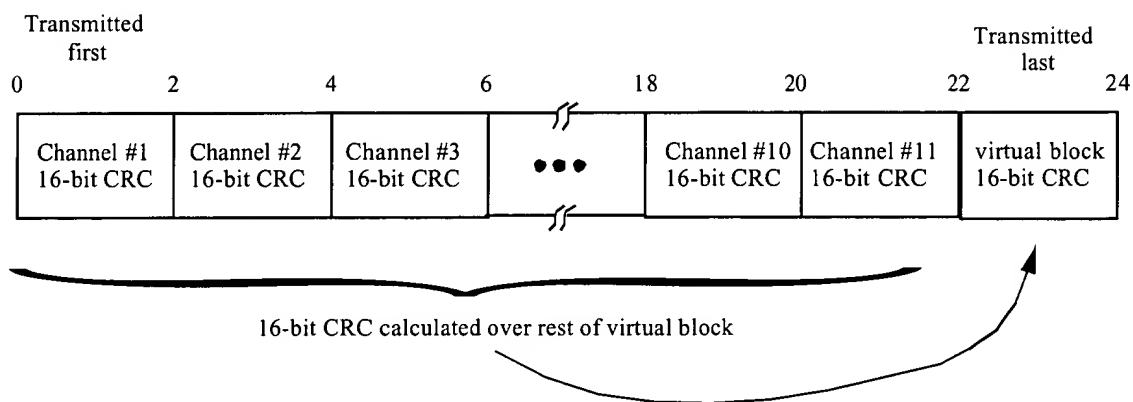


Figure 9, Error Correction Channel Format -
Composition of 24 Byte virtual block

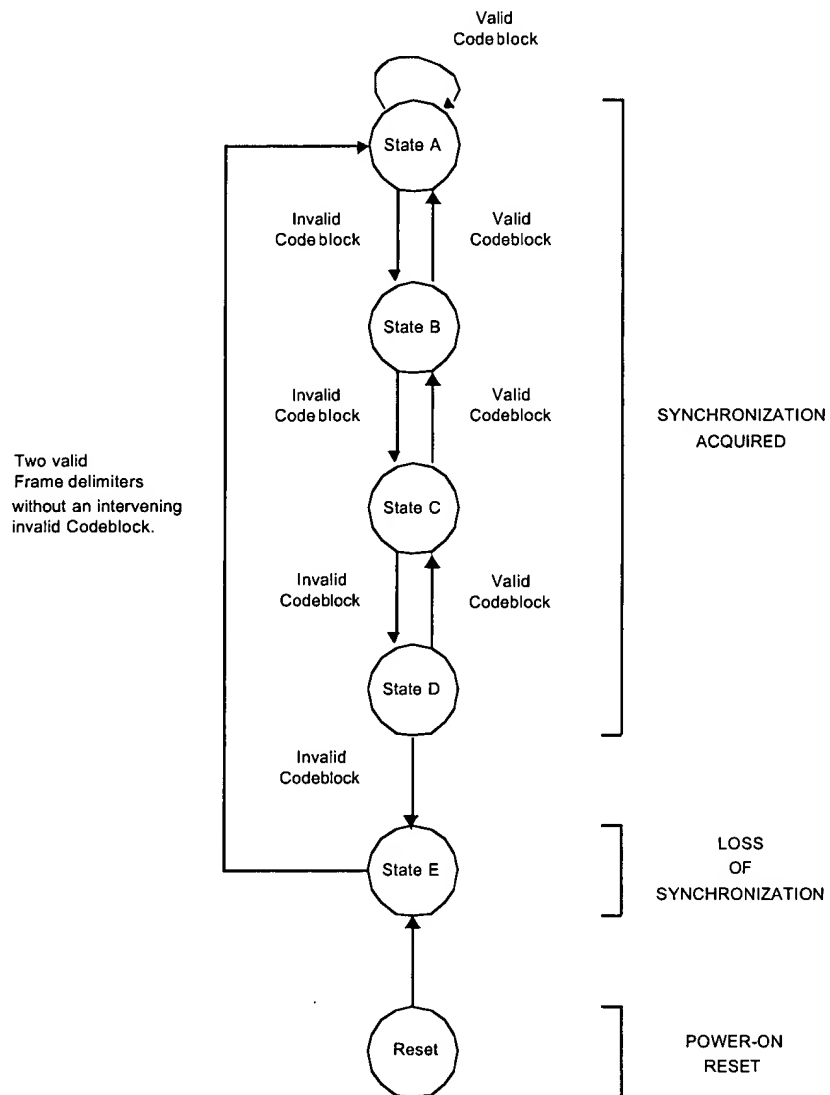


Figure 10, Loss of Synchronisation procedure (state diagram)

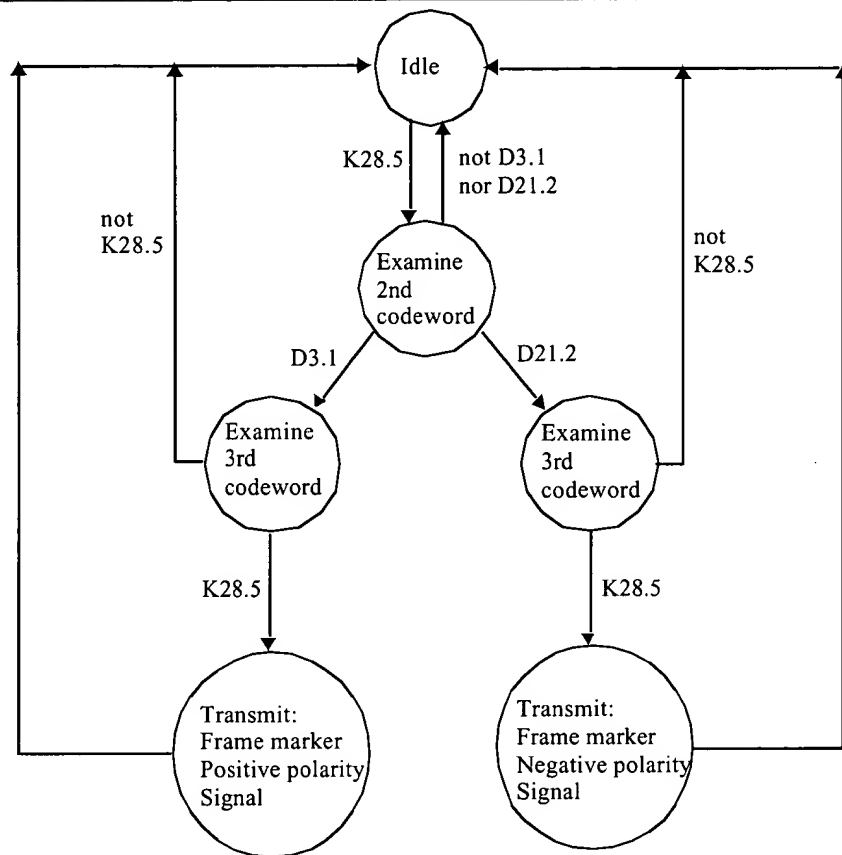


Figure 11, State diagram for detection of frame delimiter and channel polarity

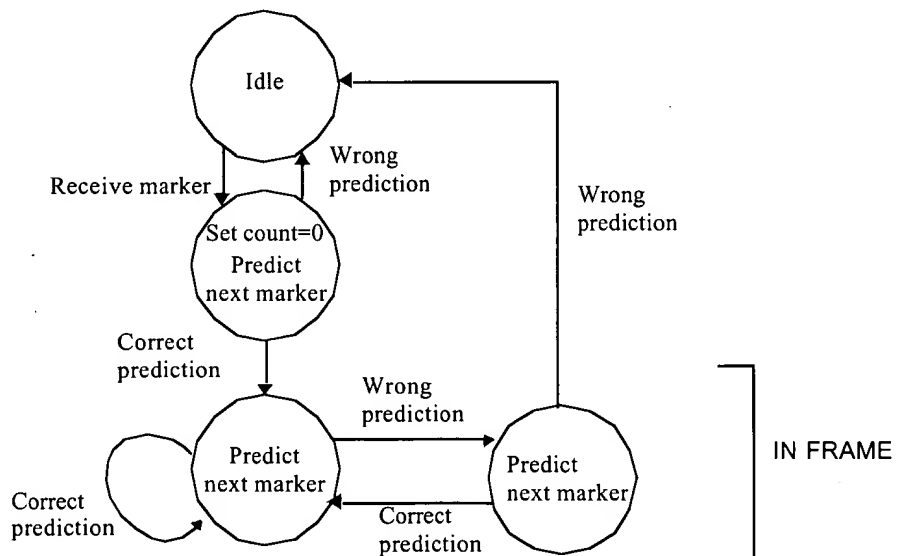


Figure 12, In frame detection state diagram

4.0 Module monitoring test access

The OC-192 Very Short Reach Interconnect Module shall provide the following monitor and control points:

Table 5: Control and monitor signals

Control signal	Pin	Use
Laser Enable/Disable	L _{EN}	Connect to V _{OL} to enable laser. V _{OH} signal disables laser.
Signal Detect	SD	Normal optical input levels to the receiver result in a logic “0” output, V _{OL} asserted. Low input optical conditions to the receiver result in a logic “1” output V _{OH} asserted.
Loss of Synchronisation	LOSyn	Normal operation results in a logic “0” output, V _{OL} asserted. LOSyn condition on any channel results in a logic “1” output V _{OH} asserted. Remains asserted for duration of LOSyn condition.
Codeword violation	CWV	No codeword violations detected results in a logic “0” output, V _{OL} asserted. Any codeword violations detected on any channel results in a logic “1” output V _{OH} asserted for a duration of 50ns.
Protection Enable/Disable	PROT _{EN}	Connect to V _{OL} to enable protection switching based on LOSyn detection. V _{OH} signal disables protection switching when LOSyn detected.
All zeros Enable/Disable	AZ _{EN}	Connect to V _{OL} to enable ‘all zero’ insertion by the byte multiplexer in the case of multiple LOSyn detection. V _{OH} signal disables ‘all zero’ insertion by the byte multiplexer in the case of multiple LOSyn detection.
Near-end loopback Enable/Disable	NE _{LOOP}	Connect to V _{OL} to enable near-end loopback. Connect to V _{OH} to disable near-end loopback.

5.0 Testing Considerations

The transceiver module shall be 100% tested for compliance to the requirement specifications

6.0 Power Supply Requirements

6.1 Module Input Voltage Supply

The transceiver module shall be capable of operation within specification when provided with a supply voltage of +3.3V +/- 10%.

The current consumption shall be less than 2.12 A

6.2 Module Power Consumption

The transceiver module shall be targeted to consume less than 7 W under all operating conditions.

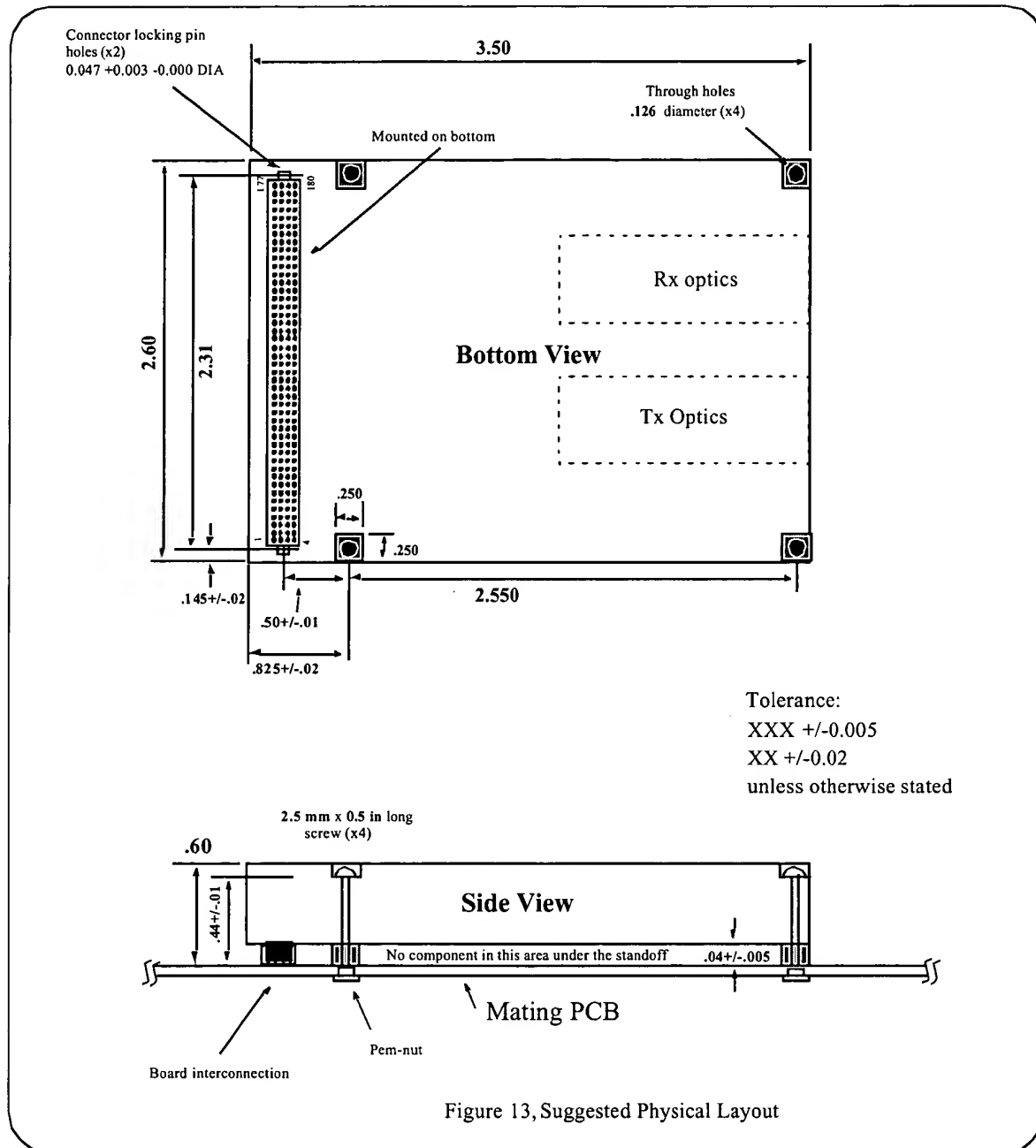
6.3 Power Supply noise rejection

The transceiver module shall perform to specifications while subjected to power rails that have broadband noise in the frequency range of 6 kHz to 2 MHz of 200 mV_{p-p}.

A printed version of this document is an uncontrolled copy.

7.0 Mechanical Description

It is desired that the transceiver module shall be contained in a package that is bound by the dimensions stated below and illustrated in Figure 13.



A printed version of this document is an uncontrolled copy.

7.1 Module Dimensions

Width: 2.6 +/- 0.05 inches

Length 3.5 +/- 0.05 inches

Height including standoffs: 0.6 +/- 0.05 inches

7.2 Optical Fiber Interface

The optical connectors for both transmit and receive optical sub-modules shall be MTP (MPO) fiber connectors capable of connecting to an MTP(MPO) terminated fiber ribbon cable. The recommended fiber type shall be 62.5/125µm or 50/125 µm multimode fiber.

7.3 Transceiver Module mounting attachment

The transceiver module shall attach to the mating PCB assembly through a high density connector. There shall be mechanical alignment pins provided to aid in the mating of the connector.

7.4 Transceiver Module standoff

The module shall have a 0.040 +/- 0.005 inch standoff beneath the module.

7.5 Transceiver Module Electrical interface

The transceiver module shall attach to the mating PCB assembly through a high density connector. The proposed connector is a Samtec (female) mounted on the module for use with a mating Samtec pin header (male) mounted on the PCB.

The proposed connector is a quad row connector with 45 pins per row. The intent is to use a common connector and pinout with this module and future modules.

The Samtec part number for the connector mounted on the module (female) is FOLC-145-02-S-Q-LC

The Samtec part number for the pin header mounted on the PCB (male) is MOLC-145-02-S-Q-LC

7.6 Transceiver Module Electrical Interface Pinout

1	V _{CC} (+3.3)	2	V _{CC} (+3.3)	3	V _{CC} (+3.3)	4	V _{CC} (+3.3)
5	V _{CC} (+3.3)	6	V _{CC} (+3.3)	7	V _{CC} (+3.3)	8	V _{CC} (+3.3)
9	V _{CC} (+3.3)	10	V _{CC} (+3.3)	11	n/c	12	n/c
13	n/c	14	Gnd	15	n/c	16	n/c
17	Gnd	18	Clk_In+	19	n/c	20	n/c
21	Gnd	22	Clk_In-	23	Gnd	24	Gnd
25	Gnd	26	D _{IN} _14+	27	D _{IN} _15+	28	Gnd
29	Gnd	30	D _{IN} _14-	31	D _{IN} _15-	32	Gnd
33	Gnd	34	D _{IN} _12+	35	D _{IN} _13+	36	Gnd
37	Gnd	38	D _{IN} _12-	39	D _{IN} _13-	40	Gnd
41	Gnd	42	D _{IN} _10+	43	D _{IN} _11+	44	Gnd
45	Gnd	46	D _{IN} _10-	47	D _{IN} _11-	48	Gnd
49	Gnd	50	D _{IN} _8+	51	D _{IN} _9+	52	Gnd
53	Gnd	54	D _{IN} _8-	55	D _{IN} _9-	56	Gnd
57	Gnd	58	D _{IN} _6+	59	D _{IN} _7+	60	Gnd
61	Gnd	62	D _{IN} _6-	63	D _{IN} _7-	64	Gnd
65	Gnd	66	D _{IN} _4+	67	D _{IN} _5+	68	Gnd
69	Gnd	70	D _{IN} _4-	71	D _{IN} _5-	72	Gnd
73	Gnd	74	D _{IN} _2+	75	D _{IN} _3+	76	Gnd
77	Gnd	78	D _{IN} _2-	79	D _{IN} _3-	80	Gnd
81	Gnd	82	D _{IN} _0+	83	D _{IN} _1+	84	Gnd
85	Gnd	86	D _{IN} _0-	87	D _{IN} _1-	88	Gnd
89	Gnd	90	Gnd	91	Gnd	92	Gnd
93	Gnd	94	D _{OUT} _14+	95	D _{OUT} _15+	96	Gnd
97	Gnd	98	D _{OUT} _14-	99	D _{OUT} _15-	100	Gnd
101	Gnd	102	D _{OUT} _12+	103	D _{OUT} _13+	104	Gnd
105	Gnd	106	D _{OUT} _12-	107	D _{OUT} _13-	108	Gnd
109	Gnd	110	D _{OUT} _10+	111	D _{OUT} _11+	112	Gnd
113	Gnd	114	D _{OUT} _10-	115	D _{OUT} _11-	116	Gnd
117	Gnd	118	D _{OUT} _8+	119	D _{OUT} _9+	120	Gnd
121	Gnd	122	D _{OUT} _8-	123	D _{OUT} _9-	124	Gnd
125	Gnd	126	D _{OUT} _6+	127	D _{OUT} _7+	128	Gnd
129	Gnd	130	D _{OUT} _6-	131	D _{OUT} _7-	132	Gnd
133	Gnd	134	D _{OUT} _4+	135	D _{OUT} _5+	136	Gnd
137	Gnd	138	D _{OUT} _4-	139	D _{OUT} _5-	140	Gnd
141	Gnd	142	D _{OUT} _2+	143	D _{OUT} _3+	144	Gnd
145	Gnd	146	D _{OUT} _2-	147	D _{OUT} _3-	148	Gnd
149	Gnd	150	D _{OUT} _0+	151	D _{OUT} _1+	152	Gnd
153	Gnd	154	D _{OUT} _0-	155	D _{OUT} _1-	156	Gnd
157	Gnd	158	Clk_Out+	159	Gnd	160	Gnd
161	Gnd	162	Clk_Out-	163	Gnd	164	n/c
165	LOSyn	166	L _{EN}	167	PROT _{EN}	168	SD
169	CWV	170	AZ _{EN}	171	NE _{LOOP}	172	n/c
173	n/c	174	n/c	175	n/c	176	n/c
177	n/c	178	n/c	179	n/c	180	n/c

A printed version of this document is an uncontrolled copy.

8.0 Environmental Considerations

8.1 Storage temperature

The transceiver module shall be capable of storage in a -40 to +85 degree celsius (non-condensing) environment, without any performance or reliability deficiencies when used.

8.2 Operating temperature

The transceiver module shall be of capable operating within specifications in either one of the two environmental modes:

- 0 to 70 degree ambient environment with 100 lfpm air flow over the top surface only (bottom will be mounted on a mating PCB and will not allow forced air flow)
- 0 to 50 degree ambient when cooled by free convection. (i.e. non-fan assisted)
- In either case whether convection or forced air, the module shall operate reliably either in a horizontal or vertical orientation.

8.3 Shock

The module shall operate within specifications while subjected to a shock of 30g, 18 ms, half sine, on all axis.

8.4 Vibration

The module shall operate within specifications while subjected to vibrations of 5g, 10-2000Hz, 6 cycles/axis.

9.0 EMI/EMC compliance

The transceiver module shall meet the current version, at the time of manufacturing, of the applicable EMI/EMC specifications for telecom and datacom equipment for North American (FCC), European (CENELEC), and Japan (VCCI) standards

9.1 ESD

The electrical input pins shall be protected against ESD with a withstand voltage of at least 2 kV (with the appropriate human body model)

9.2 Package body electrical potential

If the optical module is packaged in a containment (i.e. lid or cover), then the containment shall be connected to ground potential.

10.0 Reliability

The transceiver module shall be designed to operate within specification (at ambient temperature of 30 deg C) for a duration of 10 years with a target FITS of 150.

11.0 Warning Label

The transceiver module shall have the appropriate warning label regarding the operation of possible hazardous laser radiation.

12.0 Target Cost

The transceiver module shall be targeted to cost less than \$US 1000 in 1000 qty. by 2Q00 with a target of \$US 500 by 2Q01.

13.0 Manufacturing Information

The transceiver module shall have the appropriate information to uniquely indicate the vendor, date of manufacture, and a serial and part number.

14.0 Labelling

The optical transmitter and receiver ports shall be clearly identified and labelled.

References

- [1] IEEE 802.3, 1998 Edition Information technology--Telecommunications and information exchange between systems--Local and metropolitan area networks--Specific requirements--Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications
- [2] IEC 61754-7 Fibre Optic Connector Interfaces - Part 7: Type MPO Connector Family